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FPGA-based Architecture of Direct Torque Control

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ABSTRACT

This paper presents an optimized FPGA architecture of a DTC "direct torque control" drive of an induction motor. The proposed architecture is based on variable fixed point world size and the use ipcores in order to achieve higher sampling frequency which leads to reduce the electromagnetic torque and flux ripples. The hardware implementation was experimentally validated, the results shows the effectiveness of the hardware DTC drive implementation by the minimization of the torque and flux ripple.

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1. INTRODUCTION

Before the power electronics is introduced, induction motors were mainly used for applications with almost constant speed because of the unavailability of a variable frequency drive. The advancement of power electronics has solved this problem and extended the use of induction motors for variable speed applications, but due to the inherent linkage of flux and torque, the performance did not reaches that of the DC machine. Decades ago, the methodology field oriented control (FOC) of an induction motor was established which has opened a new horizon for induction motors applications. This methodology is based on the frames transforms (Concordia, Park, Park inverse), and the decoupling of control variables. Its major drawback is the complexity of the control algorithm which makes this solution a complex operation from implementation on an embedded target.

The direct torque control DTC (Direct Torque Control) has been proposed in 1986 by Takahashi [1], it allows the speed control through the direct control of the motor electromagnetic variables. This technique uses a simpler control structure based on estimators and hysteresis regulators, to control independently the stator flux and torque. The simplicity lies in limited vector operations and coordinates transformation, the absence of modulation operations (PWM, SVM) and the non-necessity of a position sensor.

Although its structure is simple, DTC requires a fast processor to perform electromagnetic torque and stator flux estimator computation. Different embedded solutions were investigated to achieve a high sampling frequency F_s, such as DSP [2]-[4] where its F_s can reach up to 20 kHz. However, this is not enough for the discrete hysteresis controller to reaches the same performance as analog operation, where torque and flux ripple output are limited within the hysteresis band.

Therefore, other solutions have been proposed in the literature, some studies [6], [7],[8] have used a combination of DSP and FPGA to reduce the computational load on DSP by distributing tasks to the FPGA. However, this combination of software and hardware solution increases the cost and complexity of

interfacing the circuit and is not a practical solution for commercial purposes. Other studies [9]-[11] have proposed hardware FPGA based implementation of the entire DTC algorithm where the VHDL code was generated using Xilinx system generator toolbox of Matlab, a significant amelioration of torque and flux ripple were found but the VHDL code was not optimized to achieve higher sampling frequency.

In this work, a novel FPGA implementation of DTC based on hysteresis controller is developed usinga variable fixed point world size and involving ip-cores of Xilinx to compute complex functions involved in DTC algorithm such as the square root and trigonometric functions. The performance of the proposed FPGA architecture is experimentally validated. A high sampling frequency is achieved showing a significant reduced torque and flux ripple

2. DTC ALGORITHM

The DTC essentially consists of a torque control loop and a speed control loop, as shown in Figure 1. In this topology, the stator flux and electromagnetic torque are respectively controlled by the means of a 2 level and 3 level hysteresis regulators. The outputs of comparators and the sector number are used to index the switching table "look-up-table" in order to select the appropriate switching states of the inverter switches. In this loop, the most important sub-module that can guarantee satisfactory performance of the DTC is the estimator of the stator flux and torque [12], [13].

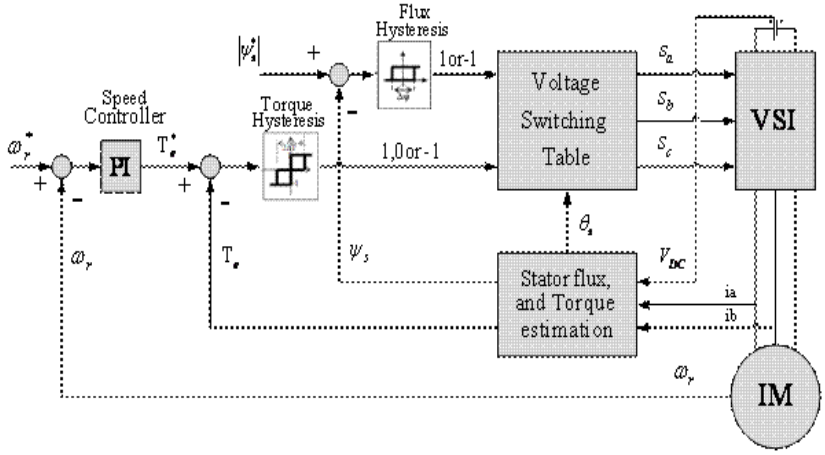

Figure 1. Modules of the DTC algorithm

The computation operations involved in the flux and torque estimator are described by the above equations:

- *(α,β) transform:*

$$\begin{cases} I_\alpha = I_a \\ I_\beta = \frac{\sqrt{3}}{3}(I_a + 2I_b) \end{cases} \quad (1)$$

$$\begin{cases} V_\alpha = \frac{V_{dc}}{3}(2S_a - S_b - S_c) \\ V_\beta = \frac{\sqrt{3}}{3}V_{dc}(S_b + S_c) \end{cases} \quad (2)$$

- *Stator flux in (α, β) frame:*

$$\begin{cases} \varphi_\alpha = \varphi_{\alpha 0} + (V_\alpha - R_s I_\alpha)T_s \\ \varphi_\beta = \varphi_{\beta 0} + (V_\beta - R_s I_\beta)T_s \end{cases} \quad (3)$$

Where T_s is the sampling period (µs) and R_s is the stator resistance (ohms).

Neglecting the stator resistance, equations 13 and 14 implies that the tip of the stator vector will move in the direction of the applied voltage vector in a straight line as indicated in Figure 2. For controlling

the amplitude of the stator flux, the voltage vector plane is divided into six regions. Each of these sectors is 60° wide. In each region, two adjacent voltage vectors may be selected to increase or decrease the stator flux amplitude and give a minimum switching frequency [14]. The switching table is given by the Table 1:

Table 1. Switching Table

φ	T	Zone 1	Zone 2	Zone 3	Zone 4	Zone 5	Zone 6
ϕ = 1	1	V_2	V_2	V_4	V_5	V_6	V_1
	0	V_7	V_0	V_7	V_0	V_7	V_0
	-1	V_6	V_1	V_2	V_3	V_4	V_5
ϕ = 0	1	V_3	V_4	V_5	V_6	V_1	V_2
	0	V_0	V_7	V_0	V_7	V_0	V_7
	-1	V_5	V_6	V_1	V_2	V_3	V_4

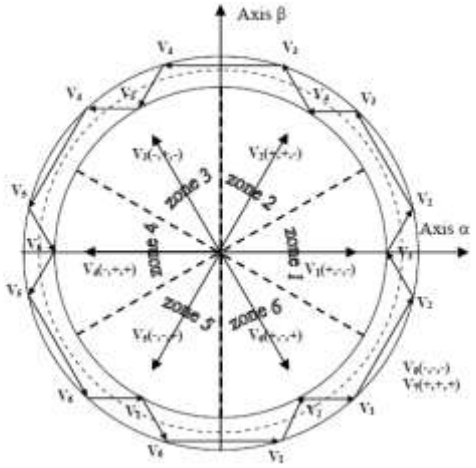

Figure 2. Selected stator voltage regrading the stator flux sector

The torque and flux hysteresis controllers select the appropriate voltage vectors. Table 1 indicate the six and eight voltage vectors switching strategies, in each region Te and φ are increasing or decreasing functions of time. When the torque is increasing or decreasing, the flux linkage can be increased or decreased by selecting alternatively one of the six non zero voltage vectors and one of the two zero voltage vectors [15][16]. The torque and flux are increased or decreased by selecting only the six non zero voltage vectors. The torque is changed by reversing the movement of the stator flux vector at each state of the hysteresis controller output [17].

●Sector number of flux vector:

$$\emptyset_s = arctg\left(\varphi_\alpha / \varphi_\beta\right) \tag{4}$$

●Torque and stator flux magnitude estimation:

$$\begin{cases} \varphi_s = \sqrt{\varphi_\alpha^2 + \varphi_\beta^2} \\ T_e = \frac{3}{4} P(I_\beta \varphi_\alpha - I_\alpha \varphi_\beta) \end{cases} \tag{5}$$

Where *P* is the pole's number of the induction motor, T_e *is* the electromagnetic torque (N.m) and φ_s is the stator flux magnitude (Wb). The flux 2-level hysteresis controller, as depicted in Figure 3, is described by the following equations:

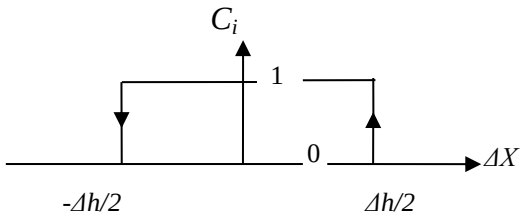

Figure 3. 2-level hysterisis satates

$$\begin{cases} C_i = 1 & if \;\; \Delta X = (X_{ref} - X_{mes}) \geq \Delta h/2 \\ C_i = 0 & if \;\; \Delta X = (X_{ref} - X_{mes}) \leq \Delta h/2 \end{cases} \quad (6)$$

Where C_i is the control inverter control signal, and Δh is the hysteresis band.
The torque 3-level hysteresis controller is described by the following equations:

$$\begin{cases} C_i = 1 \;\; if & \Delta X \leq -\Delta h/2 \\ C_i = 0 \;\; if & -\frac{\Delta h}{2} \leq \Delta X \leq \frac{\Delta h}{2} \\ C_i = -1 \;\; if & \Delta X \geq \Delta h/2 \end{cases} \quad (7)$$

3. FPGA BASED ARCHITECTURE

3.1. Electromagnetic torque and stator flux estimator architecture

The major important module in DTC drive is the flux and torque estimator which involves different computational operations such as basic arithmetic binary addition, subtraction, multiplication. Other more complex calculation operations are also involved such as trigonometric functions and the square root computation, these operators add more complexity to the stage of implementation during which the performance and used FPGA resources are of major importance. In this work, the estimator is implemented in two pipelined stages as shown in Figure 4.

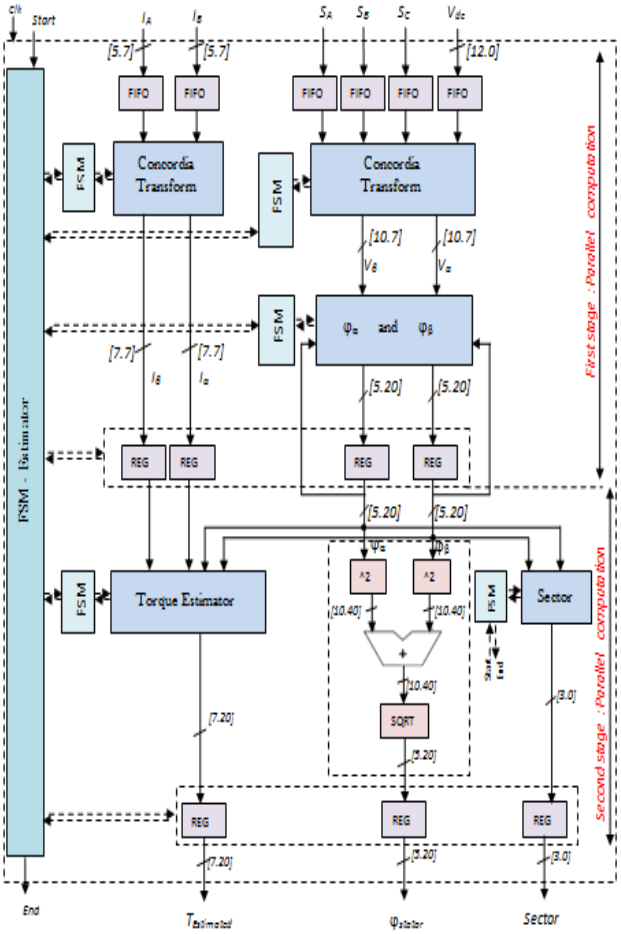

Figure 4. Architetcure of flux and torque estimator

The implementation of the estimator is performed using the two's complement fixed point format throughout the operations involved in the calculation algorithm with the exception of the operation of the square root. In this particular case, the numbers are represented in unsigned fixed point format as operand and the results are always positive.

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Determining the number of bits allocated to a variable is one of the critical points in the implementation on FPGA. First, the use of an insufficient number of bits can reduce the precision and cause a calculation error, which can destabilize the overall system. On the other hand, may increase the over sizing of the hardware implementation surface such as the case when using floating pint format. In this work, the architecture is implemented using a variable fixed-point format depending on the mathematical operation to be performed.

The square root function and the "*arctg*" function involved in the stator flux magnitude and sector computation are performed by ipcores which are pre-optimized modules from timing and resources consumption point view. The estimator is implemented in two pipelined stages; In the first stage, the Concordia transform of stator currents and voltages as well as the stator flux in *(α,β)* frame are performed in parallel computation. In the second stage, the estimated torque, the estimated stator flux magnitude, and the sector number computation are performed in parallel. The two sequential stages are synchronized using a number of registers. Different estimator operations are controlled by a local finite state machine FSM.

3.2. FPGA Architecture of the DTC

The FPGA architecture of the DTC algorithm is described in Figure 5. At the time tk, DTC control sequencer is activated by the start signal at a high logic level, it triggers sequentially the digital analog conversion and the internal sequencer of the DTC. Initially Concordia transform and the PI controller are activated in parallel, these modules generate the values of Iα , Iβ , Vα and Vβ as well the torque reference value. After the estimator computation the sector position and the hysteresis controller are activated. Errors sates on the flux and torque are compared to the hysteresis band at the end of each computation cycle; the control pulses (S1, S2, S3) are generated and applied to the switches of the DC-AC inverter.

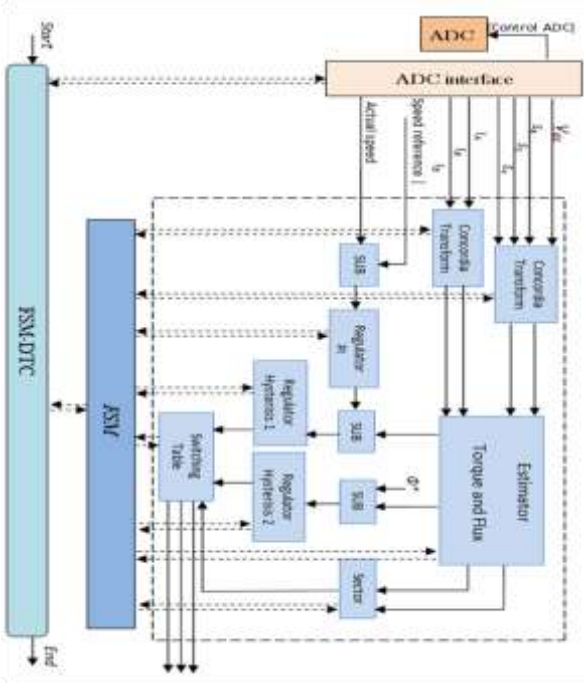

Figure 5. DTC architetcure

4. FPGA SYNTHESIS RESULTS

The FPGA synthesis results on Spartan-3E FPGA (XC3S500E-4FG320C) are presented in Table.2 and Table 3 as follow:

Table 2. Ressources utilization summary

Resources utilization	
Slices number	970 (21%)
LUTs Number	1153 (13%)
Mult (18×18)	2(10%)

Table 3. FPGA computation performance

Module	Latency	Execution Time
ADC	120	2.4 µs
Speed encoder	2	0.04 µs
abc-αβ	4	0.08 µs
Estimator : Teand Flux	6	0.12 µs
Sector position	4	0.08 µs
Switching Table	4	0.08 µs
Hysterisis	3	0.06 µs
PI	6	0.12µs
$T_{DTC} = T_{\alpha\beta} + T_{Est} + T_{Secteur} + T_{Hys} + T_{PI}$		0.54 µs
$T_{total} = T_{DTC} + T_{ADC}$		3.22 µs

The implemented DTC algorithm is executed in 0.54 µs, the total necessary time for the DTC is 3.22 µs considering the analog to digital conversion.

5. EXPERIMENTAL RESULTS AND COMPARAISON

The experimental set up is described by the Figure 6. It consist of three main stages; power electronic stage (power supply, VSI), adaptation and conditioning (ADC, DAC, Amplifier, acquisition), the FPGA and the three phase induction motor with parameters are listed in Table 4.

Table 4. Induction Motor Parameters

Parameters	Values
Nominal voltage	230/400 V
Nominal current	2.8/4.5 A
Nominal Power	1.3 KW
Nominal speed	1578 rpm
Poles	2
Moment of inertia (J)	0.0038 Kg.m^2
Viscous friction coefficient	0.0032 N.m.s/rad

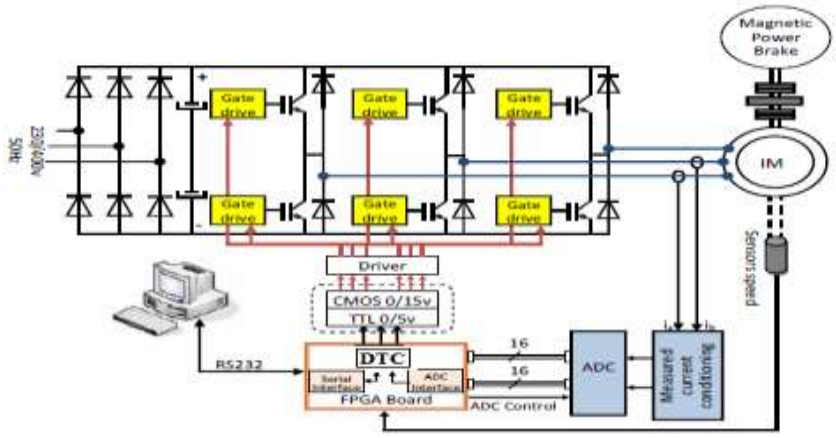

Figure 6. Schematic of the experiment set up

An experimental validation of the DTC implemented on FPGA is carried out to study the performance of the DTC FPGA-based components as well as the effectiveness of the developed hardware architecture that resulted in an execution time of 3.22 µs . Figure 8 shows the experimental results of stator flux, the reference value is 0.8 Wb and the electromagnetic torque estimated for a sampling frequency of 50 kHz and a frequency of 200 kHz.

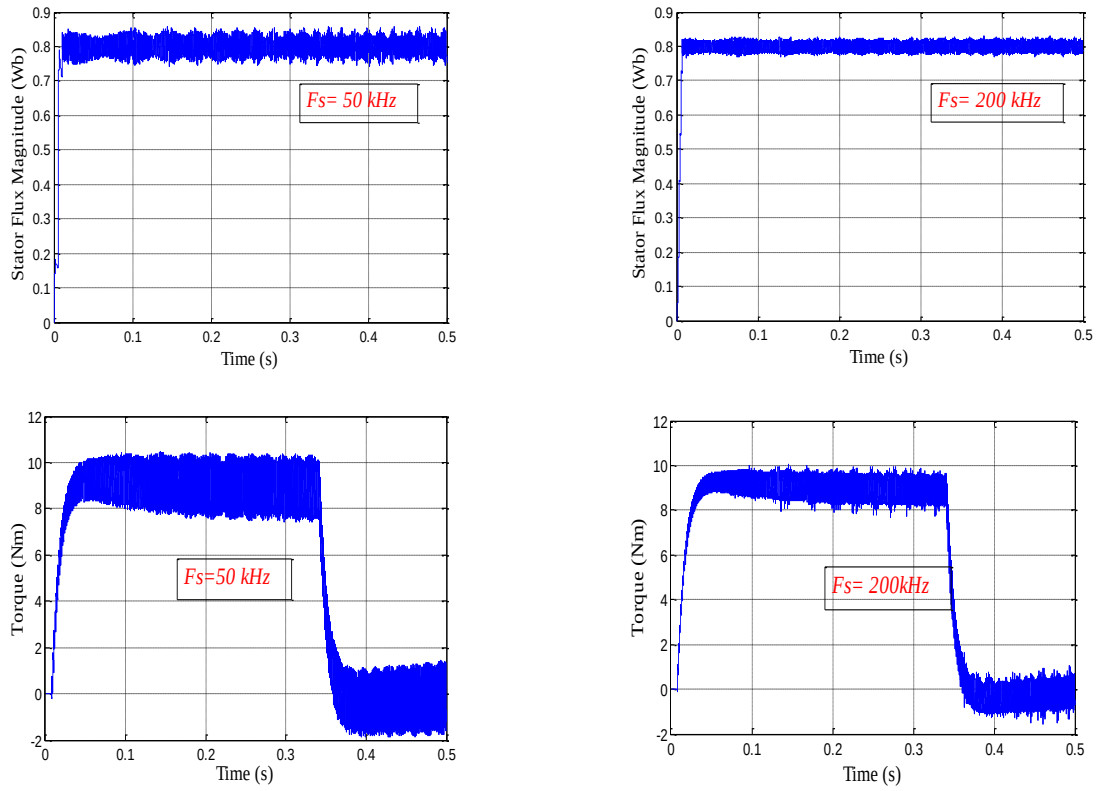

Figure 8. Stator Flux and electromagnetic torque estimated for a sampling frequency of 50 kHz and 200 kHz

Based on the experimental results of the DTC control performance is improved in terms torque ripple and stator flux when the sampling frequency increases.The torque and flux ripple achieved are respectively 12.5 % and 4.32 % showing the high performance of the proposed DTC architecture. Table 5 presents a comparaison of the proposed architecture to other works in the literature.

Table 5. Comparaison Table

Reference	Sampling frequency	DTC	Plateform	Ripple (%) Torque	Flux
Proposed	200 kHz	Hysterisis	FPGA	12.5	4.32
[18]	20 kHz	Fuzzy	FPGA Xilinx Virtex-V xc5vfx70t-3ff1136	59.64	6.37
[19]	200 kHz	Hysterisis	FPGA Altera APEX20K200EFC484-2x	9.09	2
[20]	(-)	SVM	FPGA Xilinx Spartan 3	80%	10

6. CONCLUSION

This paper presented an FPGA implementation of a DTC drive. The DTC FPGA architecture was described where the estimator was highlighted. The estimator was implemented using a variable fixed point format in order to enhance its computation performance. In addition the hardware implementation was optimized to achieve higher sampling frequency leading to reduce the torque and flux ripple. The torque and stator flux ripple achieved are respectively 12.5% and 4.32% at a 200 kHz sampling frequency. The DTC performance is enhanced with an optimized FPGA resources utilization as well an execution time of 3.22 µs considering the analog to digital conversion.

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